Equivalence Checking

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Equivalence Checking

- Given two Boolean functions, prove whether or not they are functionally equivalent.

- This talk focuses specifically on the mechanics of checking the equivalence of pairs of combinational circuits.
Types of Circuits

- **Combinational Circuit**
  - Digital circuit
  - No state-holding elements
  - No feedback loops
  - Output is a function of the current input

- **Sequential Circuit**
  - Can have state-holding elements
  - Can have feedback loops
  - Must transform (e.g. BMC) into a combinational circuit for equivalence checking
Circuit Equivalence Checking

- Checking the equivalence of a pair of circuits
  - For all possible input vectors ($2^{\text{#input bits}}$), the outputs of the two circuits must be equivalent
  - Testing all possible input-output pairs is CoNP-Hard
  - However, the equivalence check of circuits with “similar” structure is easy $^[1]$
  - So, we must be able to identify shared structure, and we need a tool that can efficiently solve NP-Complete problems (Satisfiability solver, BDDs, Gröbner Basis solver, etc.)

Equivalence Checking Uses

- **Formal Verification**
  - Prove whether a low level implementation matches a high level, or mathematical, specification

- **Verifying Compiler**
  - Maintain the functionality of generated code

- **Version Control**
  - Use previous implementations to maintain the correctness of future implementations

- **Functional Inversion**
  - Prove whether encode and decode functions are inverses of each other
Functional Verification of Hardware Design

A reasonable functional specification of any 1-bit adder:

\[
(X \Leftrightarrow (A \land \overline{B} \land \overline{C}) \lor (A \land B \land \overline{C}) \lor (A \land \overline{B} \land C) \lor (A \land B \land C)) \land \\
(Y \Leftrightarrow (A \land B) \lor (A \land C) \lor (B \land C)).
\]

A proposed implementation of a 1-bit adder:

\[
(u \Leftrightarrow (A \land \overline{B}) \lor (\overline{A} \land B)) \land \\
(v \Leftrightarrow u \land C) \land \\
(w \Leftrightarrow A \land B) \land \\
(X \Leftrightarrow (u \land \overline{C}) \lor (\overline{u} \land C)) \land \\
(Y \Leftrightarrow w \lor v).
\]

Call these formulas \(\psi_S(A, B, C, X, Y)\) and \(\psi_I(A, B, C, X, Y, u, v, w)\).

The theorem we are trying to prove is:

\[
\psi_S(A, B, C, X, Y) \Leftrightarrow \exists u, v, w : \psi_I(A, B, C, X, Y, u, v, w).
\]
Functional Verification of Hardware Design

- Given that the input variables (A, B, C) are equivalent, verify output variables (X, Y) are equivalent.
  1. Conjoin specification and implementation formulas,
  2. Add the equivalence checking constraint.
- Result –

\[
(X \Leftrightarrow (A \land \bar{B} \land \bar{C}) \lor (\bar{A} \land B \land \bar{C}) \lor (\bar{A} \land \bar{B} \land C) \lor (A \land B \land C)) \land \\
(Y \Leftrightarrow (A \land B) \lor (A \land C') \lor (B \land C')) \land \\
(u \Leftrightarrow (A \land \bar{B}) \lor (\bar{A} \land B)) \land \\
(v \Leftrightarrow u \land C') \land \\
(w \Leftrightarrow A \land B) \land \\
(X' \Leftrightarrow (u \land \bar{C}) \lor (\bar{u} \land C')) \land \\
(Y' \Leftrightarrow w \lor v) \land \\
(((X \oplus X') \lor (Y \oplus Y'))) .
\]

This is called a “miter” formula. If unsatisfiable, the specification and implementation are equivalent. A SAT solver can tell us this.
Example: Are These Circuits Equivalent?

#1

#2
Example: Outline

- **Random Simulation** -
  - Send random vectors through the two circuits, collecting pairs of candidate equivalent nodes

- **And/Inverter Graph** -
  - Find more equivalent nodes by creating the AIG of the circuits

- **SAT Sweeping** -
  - Use candidate equivalent nodes to guide SAT searches, merging AIG nodes which reduces the complexity of future SAT searches
Identifying Shared Structure

- An internal node in the first circuit may be equivalent to an internal node in the second circuit

- Detect by using random simulation
  - Percolate random vectors through both circuits (fast trick - use 64-bit words)
  - Partition nodes into equivalence classes
  - This can detect potentially many, high probability, candidate equivalent nodes
Random Simulation

#1

a
b
c

#2

a
b
c
Random Simulation

Random Vector: \{a=T, b=T, c=T\}

Buckets

#1

#2

Random Vector: \{a=T, b=T, c=T\}
Random Simulation

Random Vector: \{a=F, b=F, c=F\}

Buckets

#1

\[
\begin{array}{c}
\text{a} \\
\text{b} \\
\text{c}
\end{array}
\]

\[
\begin{array}{c}
A \\
A \\
A
\end{array}
\]

\[
\begin{array}{c}
0 \\
4 \\
1 \\
2 \\
3 \\
5 \\
6 \\
7 \\
8
\end{array}
\]

#2

\[
\begin{array}{c}
\text{a} \\
\text{b} \\
\text{c}
\end{array}
\]

\[
\begin{array}{c}
O \\
O \\
A
\end{array}
\]

\[
\begin{array}{c}
1 \\
2 \\
3 \\
4 \\
5 \\
6 \\
7 \\
8
\end{array}
\]
Random Simulation

Random Vector: \{a=F, b=F, c=T\}

Buckets

1,4
7,8
2,6
3,5
Random Simulation

Random Vector: \{a=T, b=T, c=F\}

Buckets

<table>
<thead>
<tr>
<th>Bucket</th>
</tr>
</thead>
<tbody>
<tr>
<td>7,8</td>
</tr>
<tr>
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Identifying Shared Structure

- Random simulation is probabilistic
- And/Inverter Graph (AIG) \[^2\]
  - Simple data structure used to represent combinational circuits
  - Operations are fast (add node, merge nodes)

And/Inverter Graph

#1

#2
Use the AIG data structure to store circuits
- AIG can quickly add nodes and merge equivalent nodes
- Structural hashing is used
- Merging a pair of equivalent nodes can cause other nodes to be merged automatically, without need for a SAT proof
And/Inverter Graph

- Nodes represent AND gates
- Edges represent inputs to an AND gate
- Edges may be inverted
- OR gates must be converted to AND gates during AIG creation
And/Inverter Graph

#2

a
b
c

1 2

3

A

8

y
And/Inverter Graph

#2

a
b
c

1 2

3

8

y
And/Inverter Graph

#1

#2
And/Inverter Graph

#1

0

#2

a
b
c

A

x

y

0 1 2 3 4 5 6 7 8
And/Inverter Graph

#1

#2

a
b
c

A

A

x

y

0
And/Inverter Graph

#1

#2

a
b
c

A

A

0

1

2

3

4

5

6

7

8

x

y
And/Inverter Graph

#1

#2

a
b
c

x

y

0
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SAT Sweeping

- Use SAT to prove whether or not the candidate equivalent nodes, from the random simulation phase, are equivalent
- The candidate equivalent nodes are used as cut points
- Generate SAT problems that are solved from inputs to outputs using the candidate equivalent nodes as a guide \[^3\]

SAT Instances

- Create one SAT instance for one (or more) pair of candidate equivalent nodes
- A SAT instance encodes a miter circuit
- Each SAT search can result in the merger of equivalent AIG nodes, reducing the complexity of the AIG
And/Inverter Graph

#1

#2

a
b
c

x
y

0

1 2 3 4 5 6 7 8

#1

#2
Equivalences

Buckets

7 \equiv 8

2 \equiv 6

3 \equiv 5
SAT Solver Says 3 = 5

Buckets

7 = 8
2 = 6
3 = 5
Merge 3 and 5

Buckets

7 ?= 8
2 ?= 6
3 = 5
SAT Solver Says 2 = 6

Buckets

7 ?= 8
2 = 6
3 = 5
Merge 6 and 2

Buckets

7 \approx 8

2 = 6

3 = 5
7 Structurally Hashes to 8

Buckets

- 7 = 8
- 2 = 6
- 3 = 5
x and y Verified Equivalent

<table>
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Equivalence Checking in the Large

$\text{shared input variables}$

$\text{common structure}$

$\text{equivalent ?}$

$\ f \ $ $\ f_{\text{optimized}} \ $
Equivalence Checking in the Large

Slides taken from A. Biere. SAT in Formal Hardware Verification.
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$\text{shared input variables}$

$\text{f}$

$\text{f_{optimized}}$

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\[ f = f_{\text{optimized}} \]

shared input variables

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Cryptol

- Cryptol is a Haskell based specification language for writing crypto-algorithms
- Created by Galois Connections Inc. with support from NSA cryptographers
- Cryptol specifications can be transformed into AIGs
  - Cryptol also has a built in equivalence checker (jaig)
- Cryptol specifications can be used to verify various implementations
  - C code, VHDL, etc.
Results - AES

- Verified Cryptol specification of full rank AES-128 functionally equivalent to NIST competition optimized C-code
  - Cryptol-AES AIG has 934,000 nodes
  - NIST-AES AIG has 1,482,000 nodes
  - 190,000 equivalent nodes found
  - Using techniques described here plus special SAT heuristics
    - < 1 minute on 2 GHz Pentium III
Results - VdW

- Van der Waerden numbers $W(k,r)=n$
  - Place numbers 1 ... n into k buckets so that no arithmetic progression of length r exists in any bucket
  - Assertion by Dr. Michal Kouril
    - $W(2,6) = 1132$
  - This is quite a feat because now only 6 numbers are known and no new ones had been found since 1979
Results VdW

- Dr. Kouril's solver is written in VHDL, runs on a cluster of FPGAs at UC
- The solver has exhausted the search space
- How to give confidence that VHDL code is correct?
- Use equivalence checking!
Results VdW

- Wrote Cryptol specifications for the three main VHDL functions used
- Used Xilinx tools and Cryptol to generate AIGs from the VHDL code
- Used the Cryptol equivalence checker (jaig) to verify the VHDL code
  - Each function has $2^{240}$ possible inputs
  - Total time for all three checks < 30 minutes
References


